MAHSA MEHRAD

Associate Professor

School of Engineering

Damghan University, Damghan, Iran

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EDUCATION:

- 2010-2014: **PhD**, Electrical Engineering
  Semnan University, Semnan, Iran.
  Dissertation: Lateral double diffused metal oxide semiconductor transistor: analysis and improvement characteristics
  Advisor: Prof. Ali A. Orouji

- 2012-2013: **Sabbatical leave**, Electrical Engineering
  Politecnico di Milano, Milan, Italy.
  Supervisor: Prof. Alessandro S. Spinelli

- 2008-2010: **M.Sc**. Electrical Engineering
  Semnan University, Semnan, Iran.
  Thesis: Analysis and simulation of multi-gate SOI-MOSFETs
  Advisor: Prof. Ali A. Orouji

- 2003-2007: **B.Sc**. Electrical Engineering
  Semnan University, Semnan, Iran.

Professional Experiences:

- 2018-present: **Associate Professor** at Damghan University, Damghan, Iran.
- 2015-2017: Head of Electrical and Electronic Engineering Group, Damghan University, Damghan, Iran.
- 2014- 2017: **Assistant Professor** at Damghan University, Damghan, Iran.

Honors and awards:

- Member of national elite foundation in Iran.
- Distinguished researcher, Damghan University, Damghan, Iran, 2016.
- 2014: Ranked first among all Ph.D students in Electrical and Computer Engineering Department, Semnan University, Semnan, Iran.
- 2010: Ranked first among all participants of Ph.D exam in electronic engineering, Semnan University, Semnan, Iran.
- 2010: Ranked first among all M.Sc students in Electrical and Computer Engineering Department, Semnan University, Semnan, Iran.
- 2010: Distinguished researcher, Semnan University, Semnan, Iran.

Reviewer and Editor

- 2017-present: Editorial board member of AEU-International Journal of Electronics and Communications, Elsevier
- Reviewer in more than 20 ISI journals

RESEARCH INTERESTS:

- Semiconductor devices
- Micro and nano electronic
- Transistors
- Silicon on insulator technology
- Power electronic devices
- Field Effect Transistors
- Device fabrication

SCHOLARSHIPS:

- 2011-2014: PhD scholarship from Iranian ministry of science, research and technology

TEACHING EXPERIENCE:

- **Damghan University, school of Engineering, Damghan, Iran**
  - Circuit analysis

- Physics of semiconductor
- Electronic

- **Semnan University**, Electrical and Computer Department, Semnan, Iran
  - Circuit analysis
  - Electronic I
- **Azad University of Garmsar,** Electrical Department, Garmsar, Iran
  - Electronic I
  - Electronic II
  - Logic Circuit
  - Circuit analysis
- **Azad University of Damghan,** Electrical department, Damghan, Iran
  - Physics of semiconductor devices (graduate course)
  - Technical English
  - TV system

SELECTED PUBLICATION:

Journal Papers:

1. **M. Mehrad, "**Inserting different charge regions in power MOSFET for achieving high performance of the electrical parameters**"***Silicon*, In press.

2. M. Zareiee, **M. Mehrad**, "A Reliable Nano Device with Appropriate Performance in High Temperatures," *ECS Journal of Solid State Science and Technology*, vol. 6, pp. M50-M54, 2017.

3. **M. Mehrad**, "Application of N+ Buried Layer in Reducing Lattice Temperature of Nano-Scale MOSFET," *ECS Journal of Solid State Science and Technology*, vol. 5, pp. M158-M162, 2017.

4. **M. Mehrad**, M. Zareiee, A.A. Orouji, "Controlled Kink Effect in a Novel High-Voltage LDMOS Transistor by Creating Local Minimum in Energy Band Diagram," *IEEE Transactions on Electron Devices*, vol. 64, pp. 4213-4218, 2017.
5. **M. Mehrad**, "Improved Device Performance in Nano Scale Transistor: An Extended Drain SOI MOSFET," *ECS Journal of Solid State Science and Technology*, vol. 5, pp. M74-M77, 2016.

6. **M. Mehrad**, "Reducing Floating Body and Short Channel Effects in Nano Scale Transistor: Inserted P+ Region SOI-MOSFET," *ECS Journal of Solid State Science and Technology*, vol. 5, pp. M88-M92, 2016.

7. **M. Mehrad**, "Periodic trench region in LDMOS transistor: A new reliable structure with high breakdown voltage," *Superlattices and microstructures*, vol. 91, pp. 193-200, 2016.

8. M. Zareiee, A.A. Orouji, and **M. Mehrad**, "A novel high breakdown voltage LDMOS by protruded silicon dioxide at the drift region", *Journal of Computational Electronics*, pp.1-8, 2016.

9. **M. Mehrad,** "Omega shape channel LDMOS: a novel structure for high voltage application," *Physica E*, vol. 75, pp. 196-201, 2016.

10. **M. Mehrad**, "Thin layer oxide in the drift region of laterally double-diffused metal oxide semiconductor on silicon-on-insulator: A novel device structure enabling reliable high-temperature," *Material Sci. in Semiconductor Processing,* vol. 30, pp. 599-604, 2015.

11. **M. Mehrad**, A.A. Orouji, M. Taheri, "A new technique in LDMOS transistors to improve the breakdown voltage and the lattice temperature," *Material Sci. in Semiconductor Processing*, vol. 34, pp. 276-280, 2015.

12. **M. Mehrad**, "Controlling floating body effect in high temperatures: L-shape SiGe region in nano-scale MOSFET," *Superlattices and Microstructures*, vol. 85, pp. 573-580, 2015.

13. A.A. Orouji, and **M. Mehrad**, "Positive charges at buried oxide interface of RESURF: an analytical mosel for the breakdown voltage," *Superlattices and Microstructures*, vol. 72, pp. 336-343, 2014.

14. **M. Mehrad**, and A.A. Orouji, "A novel high voltage lateral double diffused metal oxide semiconductor (LDMOS) device with a U-shape buried oxide feature," *Material Sci. in Semiconductor Processing,* vol. 16, pp. 1977-1981, 2013.

15. **M. Mehrad**, and A.A. Orouji, "Injected charges in partial SOI LDMOSs: a new technique for improving the breakdown voltage," *Superlattices and Microstructures*, vol. 57, pp. 77-84, 2013.

16. **M. Mehrad**, and A.A. Orouji, "New trench gate power MOSFET with high breakdown voltage and reduced on-resistance using a SiGe zone in drift region," *Current Applied Physics*, vol. 12, pp. 1340-1344, 2012.

17. A.A. Orouji, and **M. Mehrad**, "Breakdown voltage improvement of LDMOSs by charge balancing: an inserted p-layer in trench oxide (IPT-LDMOS)," *Superlattices and Microstructures*, vol. 51, pp. 412-420, 2012.

18. A.A. Orouji, and **M. Mehrad**, "The best control of parasitic BJT effect in SOI-LDMOS with SiGe window under channel," *IEEE Trans. Electron Devices*, vol. 59, pp. 419-425, 2011.

19. A.A. Orouji, and **M. Mehrad**, "A new rounded edge fin field-effect transistor for improving self-heating effects," *Japanese Journal of Applied Physics*, vol. 50, pp. 124303-124306, 2011.

20. **M. Mehrad**, and A.A. Orouji, "A new nanoscale and high temperature field-effect transistor: bi level FinFET," *Physica E: Low-dimensional sys. and Nanostructures*, vol. 50, pp. 124303-124308, 2011.

21. **M. Mehrad** and A.A. Orouji, "Partially cylindrical fin field-effect transistor: a novel device for nanoscale applications," *IEEE Trans. Device and Materials Reliability*, vol. 10, pp. 271- 275, 2010.

Conference Papers:

1- **M. Mehrad, "**Three p-silicon layers in reliable lateral double diffused metal oxide semiconductor transistor" Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (ULIS),Granada, Spain, 2018.

2- **M. Mehrad**, "C-shape silicon window nano MOSFET for reducing the short channel effects" Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (ULIS),Athens, Greece, 2017.

3- **M. Mehrad**, M. Zareiee, "A New Step Trench LDMOS Transistor for High Breakdown Voltage and Low Temperature Applications," in the The 24th Iranian Conference on Electrical Engineering (ICEE 2016), Shiraz, Iran, 2016.

4- **M. Mehrad,** "Reducing lattice temperature in nano-scale mosfet with reformed buried layers," *in the 3rd International Conference on Nanotechnology (ICN2015)*, 2015.

5- M. Zareiee, **M. Mehrad**, "A novel modified buried oxide nano scale mosfet for controlling self heating effects," *in the 3rd International Conference on Nanotechnology (ICN2015)*, 2015.

6- M. Zareiee, **M. Mehrad**, "Improving the short channel effects in nano scale SOI MOSFET by extending the drain region, *in the 3rd International Conference on Nanotechnology (ICN2015)*, 2015.

7- A. A. Orouji, and **M. Mehrad**, "Three independent gates fin field effect transistor,"*International Conf. on Nano Sci. Tech. (ICONSAT)*, Mumbai, India, 2010.

8- **M. Mehrad**, and A. A. Orouji, "A novel triple graded channel surrounding gate transistor,"*International Workshop on the Physics of Semiconductor Devices*, Delhi, pp. 763-765, 2009.

9- **M. Mehrad** and A. A. Orouji, "A novel SOI-MOSFET with buried alumina gate oxide,"*IEEE-RSM Pro., Kota Bahru, Malaysia*, pp. 109-112, 2009.

TECHNICAL SKILS:

- Experience and good familiarity with Silvaco programming especially ATLAS simulator.
- Experience and good familiarity with MATLAB programming and MATLAB Toolboxes: Genetic Algorithms, Neural Networks and Fuzzy logic.
- Good familiarity with C/C++, Assembly language programming, Microsoft office and LaTex.

REFERENCES:

- Prof. A. A. Orouji
  Electrical and computer engineering department, Semnan University, Semnan, Iran.
  aliaorouji@ieee.org

- Prof. P. Keshavarzi
  Electrical and computer engineering department, Semnan University, Semnan, Iran.
  pkeshavarzi@semnan.ac.ir

- Prof. A. S. Spinelli
  Electronic and Information Department, Politecnico di Milano, Milan, Italy.
  Alessandro.spinelli@polimi.it

LANGUAGES:

- Persian (Farsi): Fluent (mother tongue)
- English: Fluent
- French: Intermediate
- Italian: Beginner